claim on this basis. Applicant respectfully submits that a specific material need not be claimed provided that "a number of ion-implantations" can be carried out. Applicant notes that a variety of materials may be subject to implantation and applicant believes that the terms in the language of claim 2 are definite.

Claim 3 recites in part that "an impurity is diffused in a region where a first resistance element is to be formed." Similar to claim 2, applicant respectfully submits that the claim language is definite and a specific material need not be claimed provided that " an impurity is diffused in a region . . ." as recited in the language of claim 3.

Claim 4 recites in part that a "silicide layer" is formed. Applicant respectfully submits that this language is definite. Applicant does not understand what part of claim 4 is not definite. Provided a "silicide layer" is formed, applicant respectfully submits that the specific method of forming the "silicide layer" need not be recited in the claim for the claim to comply with section 112.

For at least the reasons stated above, applicant respectfully submits that claims 1-4 comply with section 112.

Claims 1-4 and 15-16 were rejected under 35 U.S.C. 103(a) as unpatentable over Nagai (U.S. Patent No. 6,104,053) in view of Koo et al. (U.S. Patent No. 6,262,446) and Erdeljac et al. (U.S. Patent No. 5,489,547). Claim 1 has been amended for clarity and not in response to the 103(a) rejection. The rejection is respectfully traversed.

To establish a prima facie case of obviousness, all of the following criteria should be met. First, there should be a suggestion or motivation in the art to modify the reference or to combine reference teachings. Second, there should be a reasonable expectation of success. Third, the reference(s) must teach all the claim limitations. MPEP section 706.02(j). Applicant respectfully submits that the Examiner's citations to the art are insufficient to satisfy the three criteria above and accordingly, the rejection should be withdrawn.

The Examiner stated on page 3 of the Office Action that Nagai discloses "simultaneously forming bit line 21 and connection layer 20 . . ." Applicant notes that Nagai refers to reference number 20 as a "second electrode". Applicant respectfully submits that the Examiner does not appear to have cited any specific portion of the art that establishes that reference number 20 of Nagai refers to "a connection layer . . . which is used to electrically connect a lower electrode of

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the capacitor element and another semiconductor element" as recited in claim 1, for example.

In addition, the Examiner conceded that "Nagai fails to teach the step of simultaneously forming a storage node 25, 26 of the cell capacitor and the lower electrode of the capacitor element. . ." The Examiner then applied Koo et al. as teaching "simultaneously forming capacitor electrodes for cell capacitor in the memory area and element capacitor in the peripheral region . . ." Applicant respectfully submits that the Examiner cited no portion of the art that describes or suggests the desirability of the proposed combination. The rational given by the Examiner to support the combination was ". . . in order to reduce the process steps, complexity and cost." However, as described below, with respect to at least the combination of Nagai and Koo et al., the Examiner cited no specific portion of the art that establishes a reduction in the number of processing steps, complexity and cost. Moreover, the Examiner cited no portion of the art that establishes that the proposed combination would be desirable or successful.

Applicant notes that if the reference number 11 in Nagai is considered as a lower electrode of a capacitor element in a peripheral area, then such electrode is described as being formed at the same time as gate electrodes 10a and 10b in the memory cell area. Thus, because Nagai already forms the lower electrode simultaneously with the gate electrodes 10a and 10b, there is no reason why one of ordinary skill would seek to alter the method of Nagai to later form the lower electrode as suggested by the Examiner because no net reduction in steps would occur. Moreover, Nagai forms the lower electrode 11 from the same material as the gate electrodes 10a, 10b (polysilicon 6 and tungsten silicide 7). Nagai forms the storage nodes 25, 26 in the memory cell region from polysilicon. Thus, the combination proposed by the Examiner would also appear to change the material of the lower electrode in Nagai. Moreover, the combination proposed by the Examiner would require a significant modification in the steps of the Nagai method, in which, as seen in Nagai at Figs. 5-15, forms the lower electrode 11 of a capacitor in the peripheral area together with the gate electrodes 10a and 10b in the memory cell area (Nagai Figs. 6-7), then later forms a middle electrode 20 of the capacitor in the peripheral area together with the bit line 21 of the capacitor in the memory cell area (Nagai Figs 11-12), the later forms the storage nodes 25, 26 of the memory cell capacitor (Nagai Figs. 13-14). Modifying Nagai to form the lower capacitor electrode 11 of a capacitor in the peripheral area at the same time as storage nodes 24, 25 would require a considerable change in many of the Nagai process steps.

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The Examiner does not appear to have established that one of ordinary skill would reasonably be able to make the combination proposed by the Examiner without having to significantly change the Nagai process.

Applicant respectfully submits that the Examiner has cited no adequate description or suggestion in that art for the desirability of the combination suggested by the Examiner. The Examiner's citations to the art do not appear to establish that the proposed combination would result in fewer process steps or reduce the complexity or cost of the method.

The Examiner's additional citation to Erdeljac et al. does not overcome the deficiencies of the combination of Nagai and Koo et al. as set forth above.

Accordingly, for at least the above reasons, applicant respectfully submits that the Examiner's citations to the art fail to establish a prima facie case of obviousness. Accordingly, the rejections of claims 1-4 and 15-16 should be withdrawn.

New dependent claims 17-26 have been added. Support for the new claims may be found throughout the specification and drawings and in the original claims. It is believed that no new matter has been entered.

Attached hereto is a marked-up version of the claim changes made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Applicant respectfully submits that claims 1-4 and 15-26 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

Alan S. Raynes

Alan S. Raynes
Reg. No. 39,809
KONRAD RAYNES VICTOR & MANN, LLP
315 South Beverly Drive, Suite 210
Beverly Hills, CA 90212
Customer No. 24033

Dated: November 15, 2002

tele general: (310) 556-7983
tele direct: (310) 871-8448
facsimile: (310) 556-7984

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on November 15, 2002.

Alan S. Raynes — November 15, 2002

Alan S. Raynes — **(Date)**

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Version With Markings to Show Changes Made

The paragraph in the specification starting at page 1, line 6, was amended as follows:

Reference to Cross-Related Applications

Japanese patent application no. 2000-5335, filed January 14, 2000, is hereby incorporated by reference in its entirety. U.S. Patent Application Serial No. 09/759,665 [_____], filed on January 13, 2001, [entitled "Methods for Manufacturing Semiconductor Devices and Semiconductor Devices," invented by Hiroaki Tsugane and Hisakatsu Sato, docket no. 15.28/5628,] is hereby incorporated by reference in its entirety. U.S. Patent Application Serial No. 09/759,666 [_____], filed on January 13, 2001, [entitled "Semiconductor Devices and Methods for Manufacturing the Same," invented by Hiroaki Tsugane and Hisakatsu Sato, docket no. 15.29/5629,] is hereby incorporated by reference in its entirety. U.S. Patent Application Serial No. 09/759,715 [_____], filed on January 13, 2001, [entitled "Semiconductor Devices and Methods for Manufacturing the Same," invented by Hiroaki Tsugane and Hisakatsu Sato, docket no. 15.31/5631,] is hereby incorporated by reference in its entirety.

Claims 1-2 were amended as follows:

1. (amended) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a bit line that is a component of the DRAM and a connection layer that is located in a common layer with the bit line and which [this] is used to electrically connect a lower electrode of the capacitor element and another semiconductor element;

(b) simultaneously forming a storage node of the cell capacitor and the lower electrode of the capacitor element;

(c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

(d) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.

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2. (amended) A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is carried out simultaneously with the step (d), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

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